

Fig 1

(PRIOR ART)

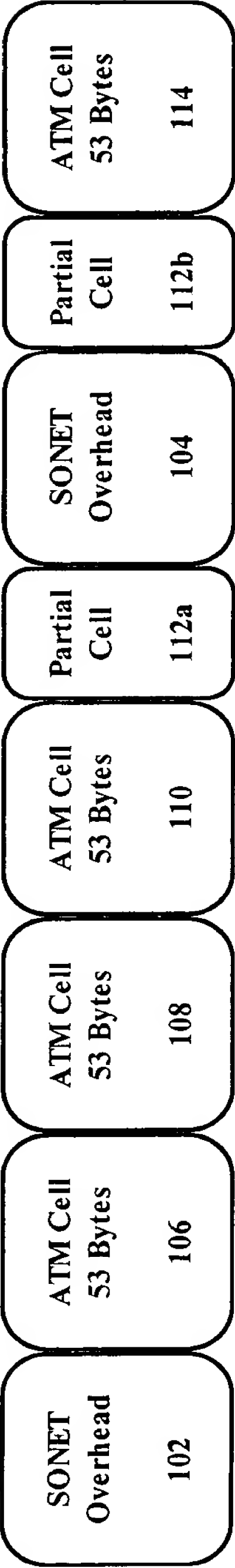


FIG. 2

Fig2

(PRIOR ART)

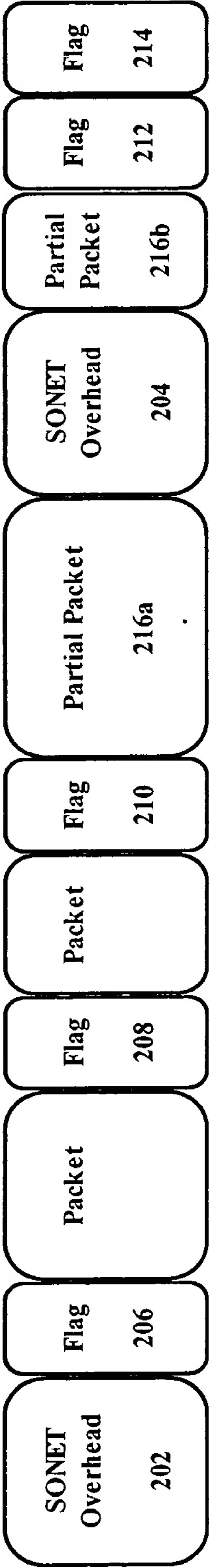


fig 3

(PRIOR ART)

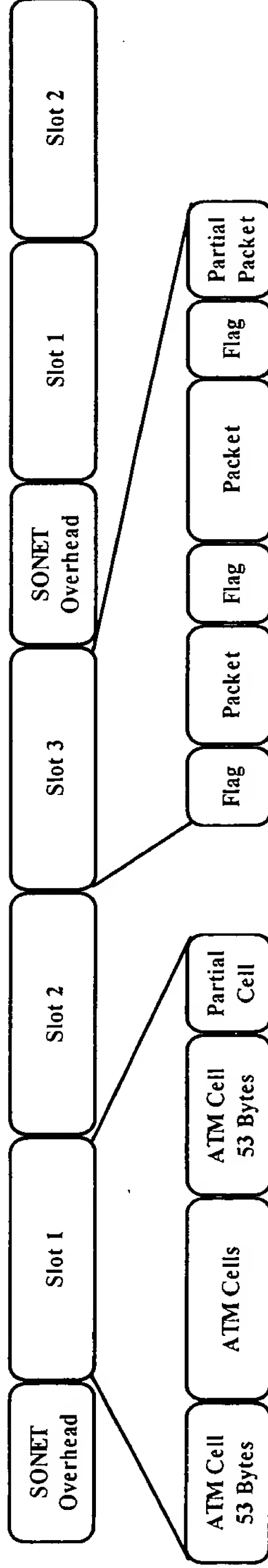
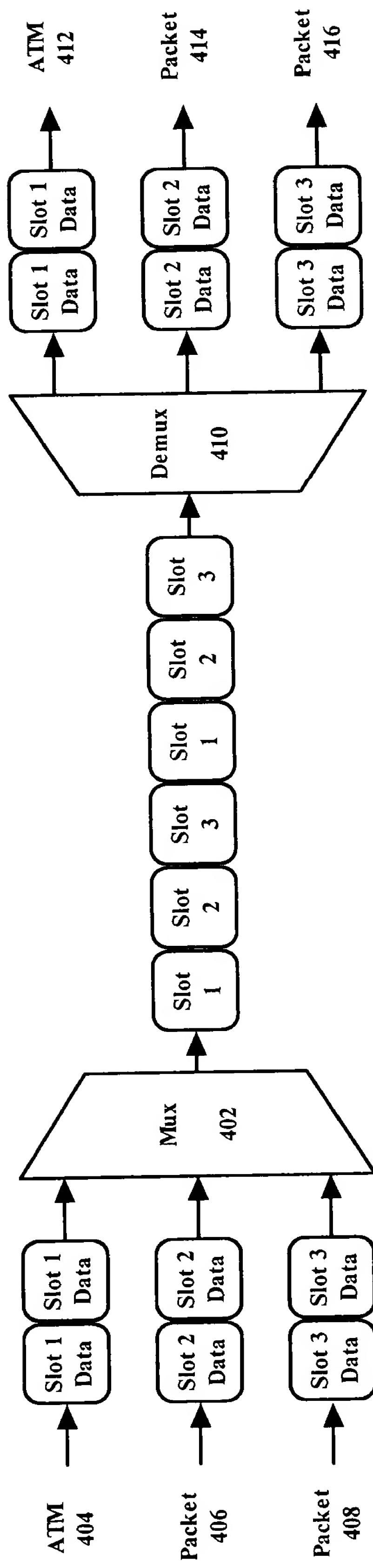


fig 4 (PRIOR ART)



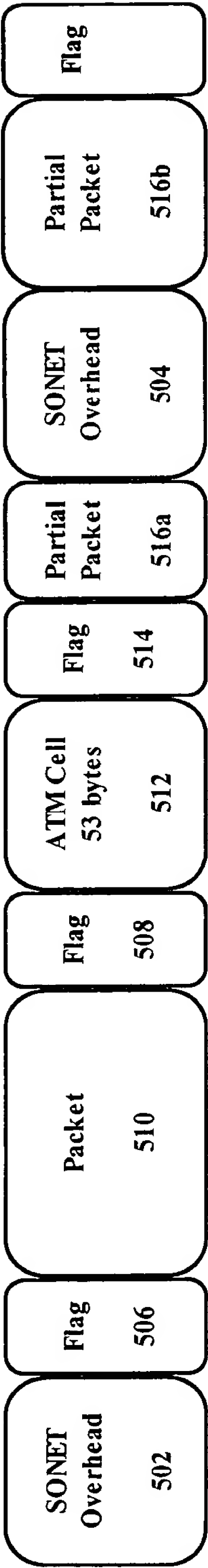


Fig. 5A

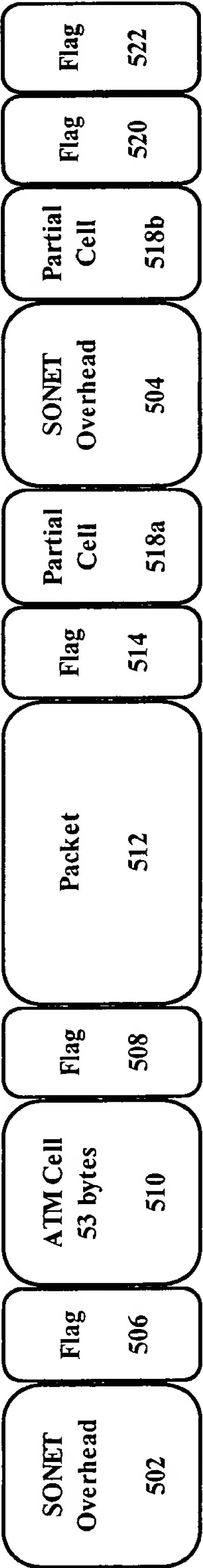


Fig. 5B

Fig 6  
(Prior ART)

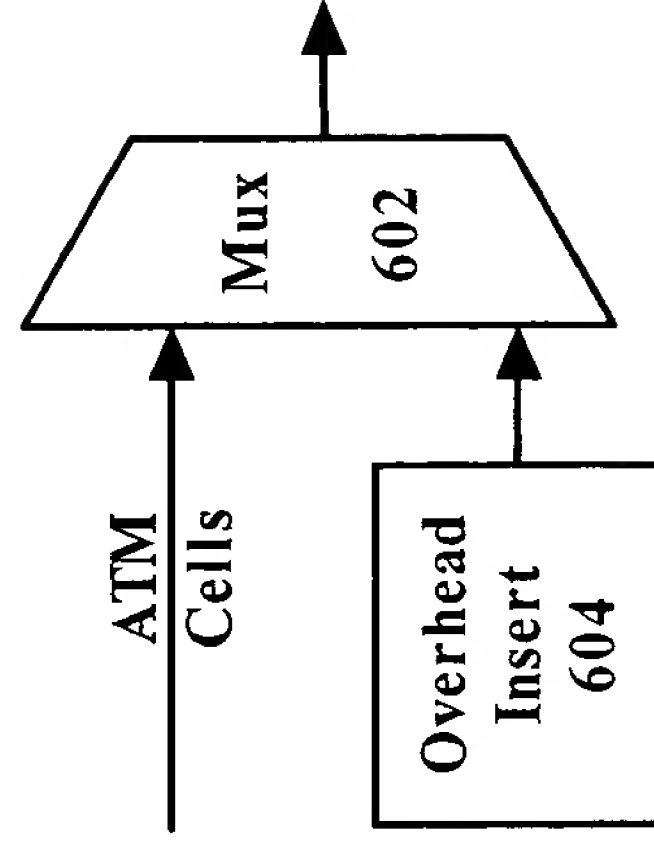


Fig 7  
(PRIOR ART)

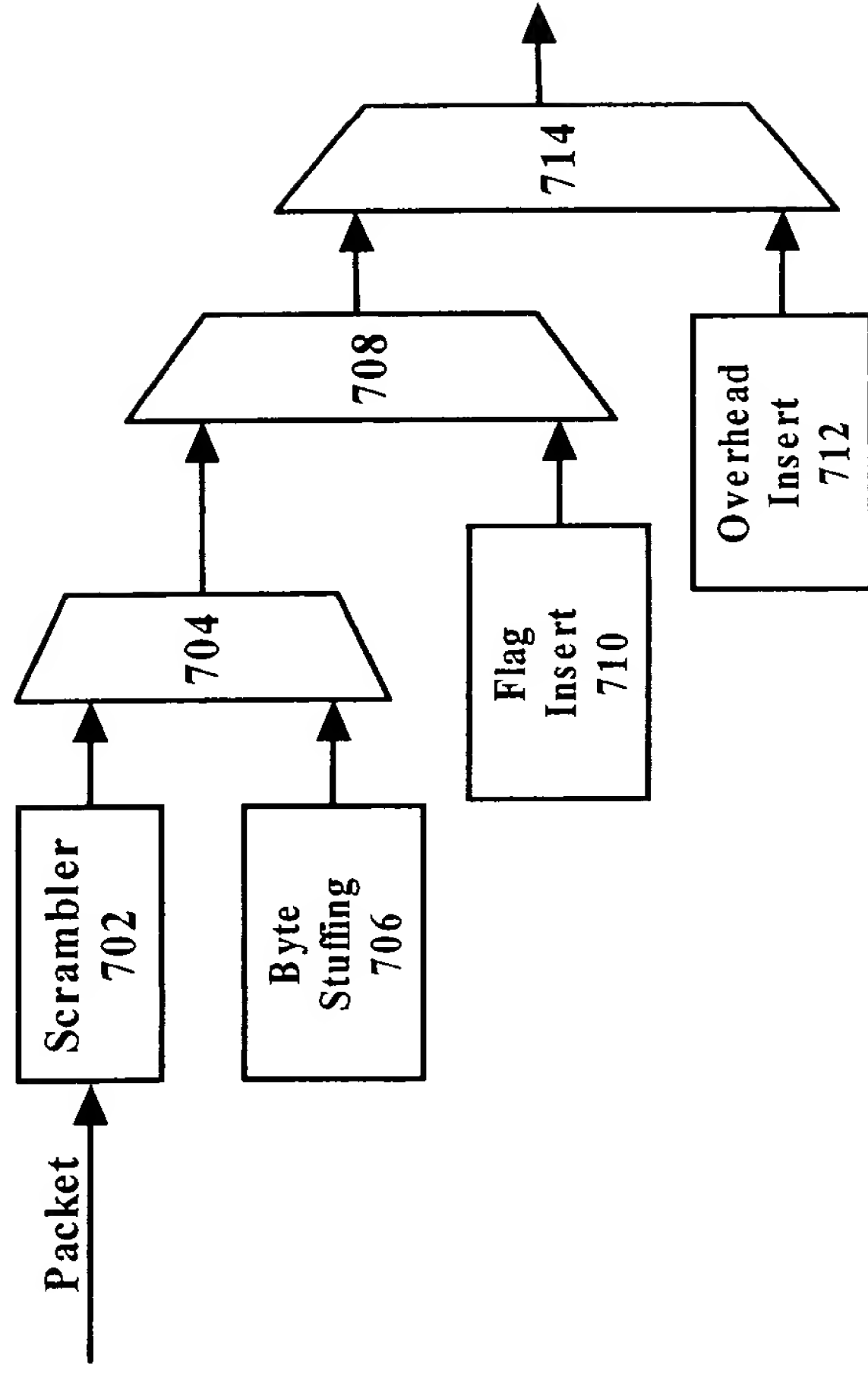
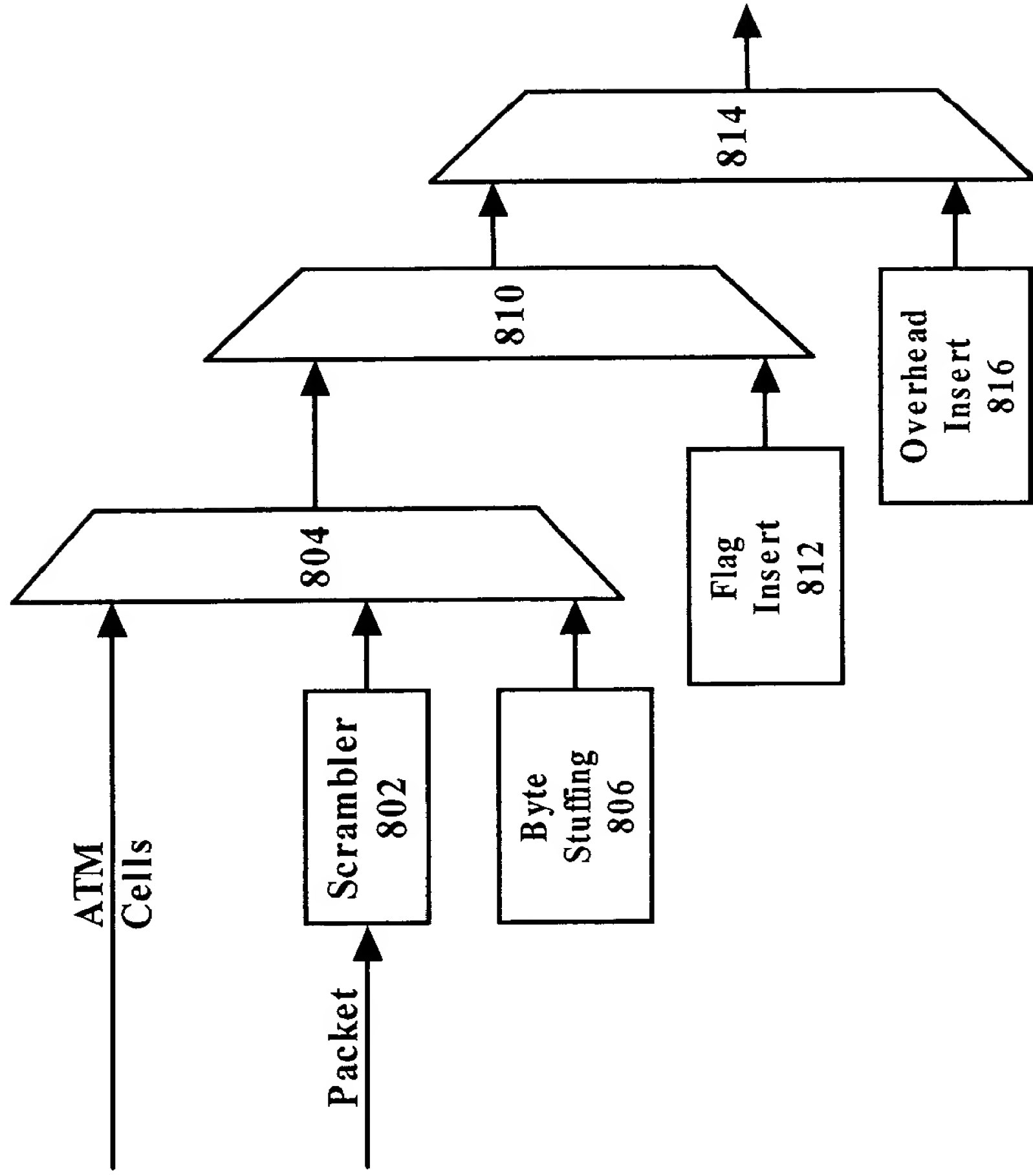


Fig 8





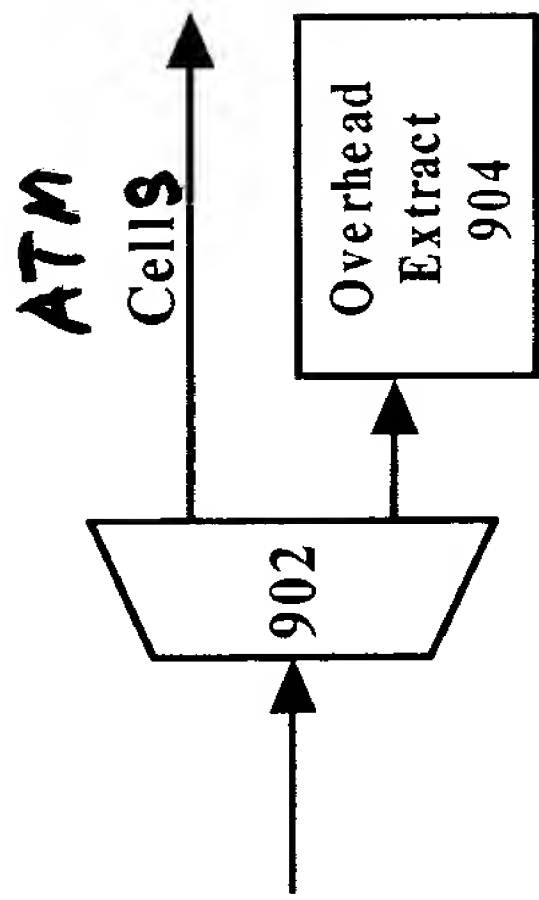


Fig. 9  
(Prior Art)

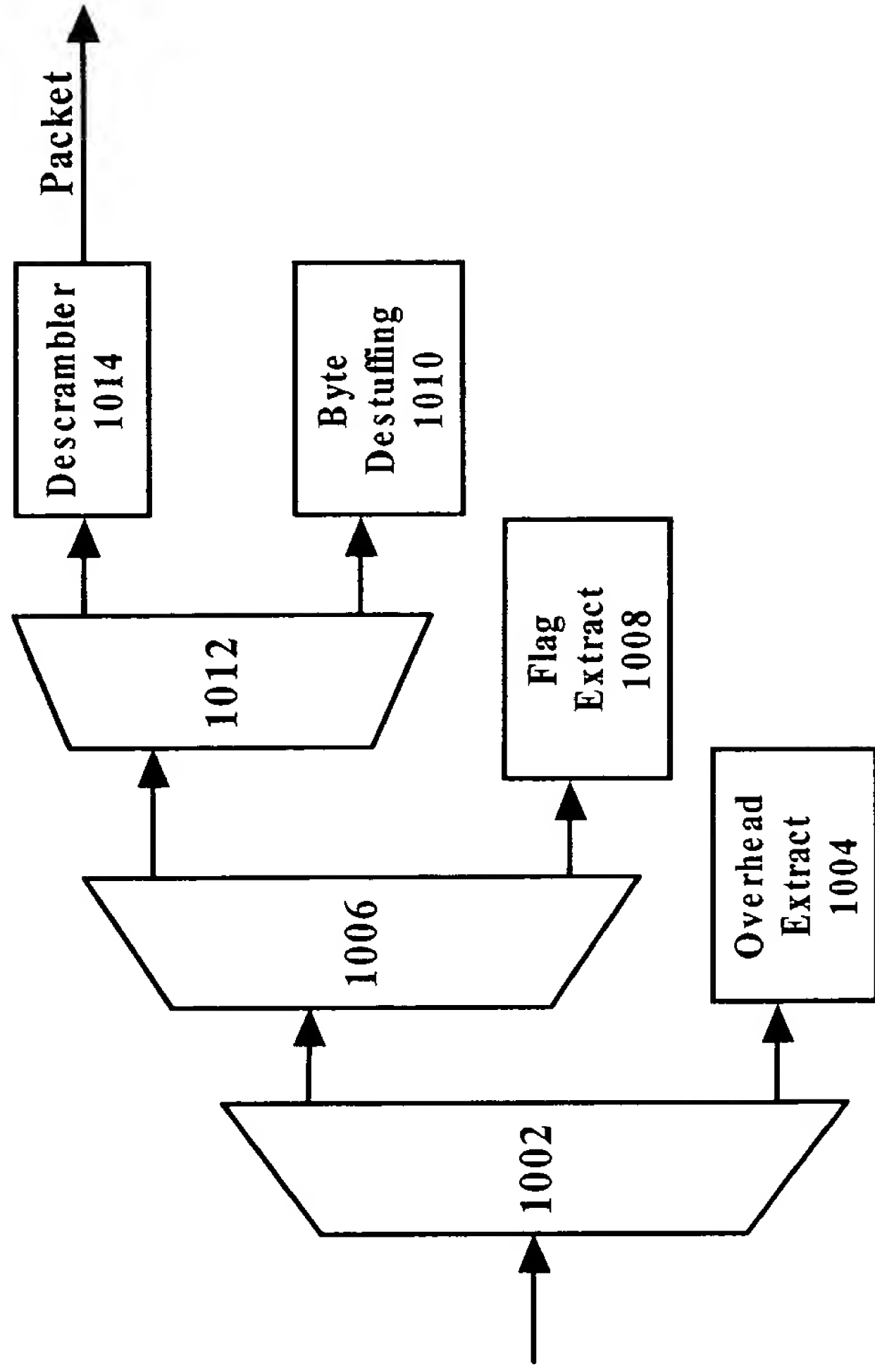


FIG. 10 (PRIOR ART)

FIG. 11 is a block diagram of a packet processing system.

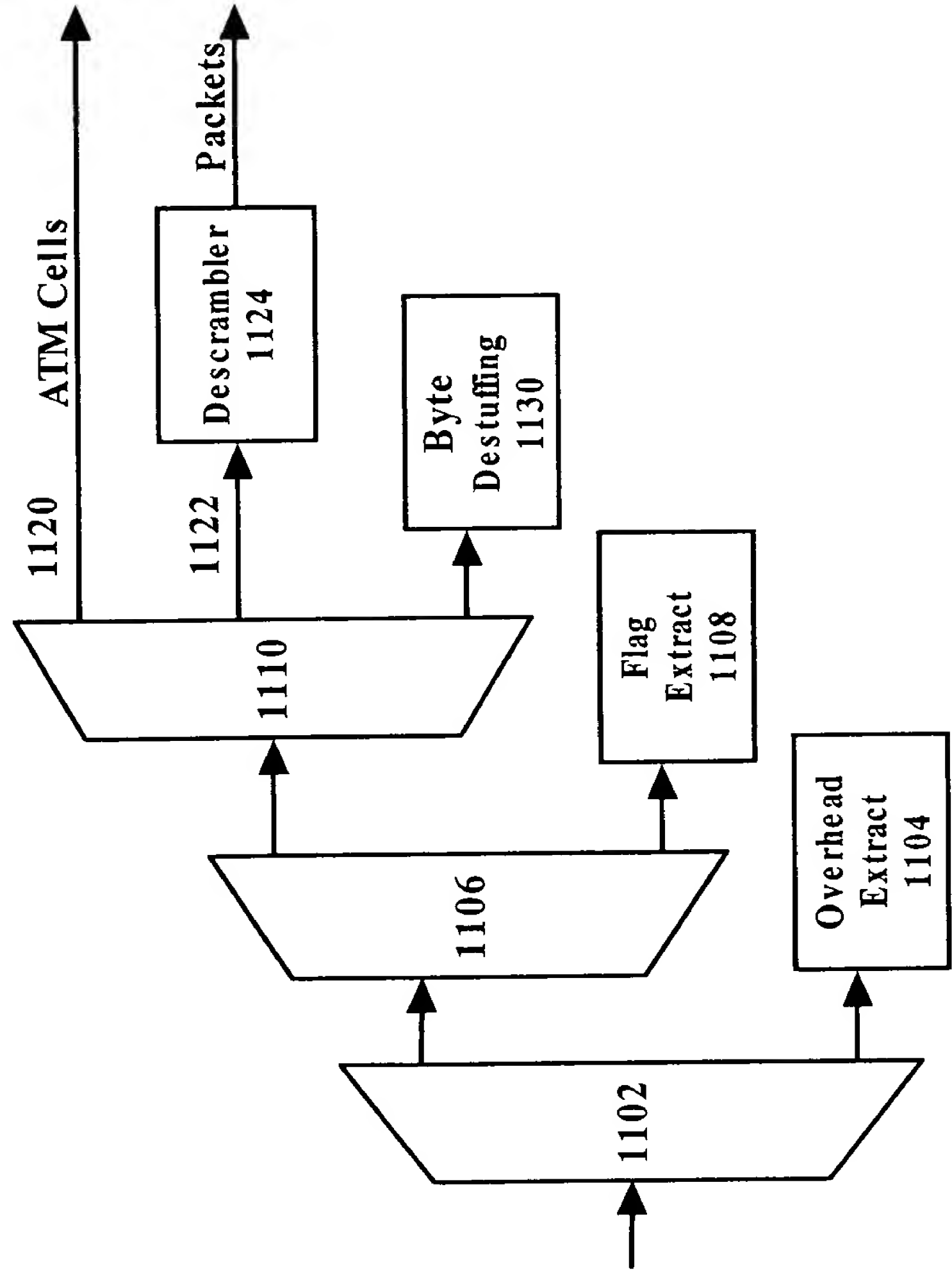


Fig. 11

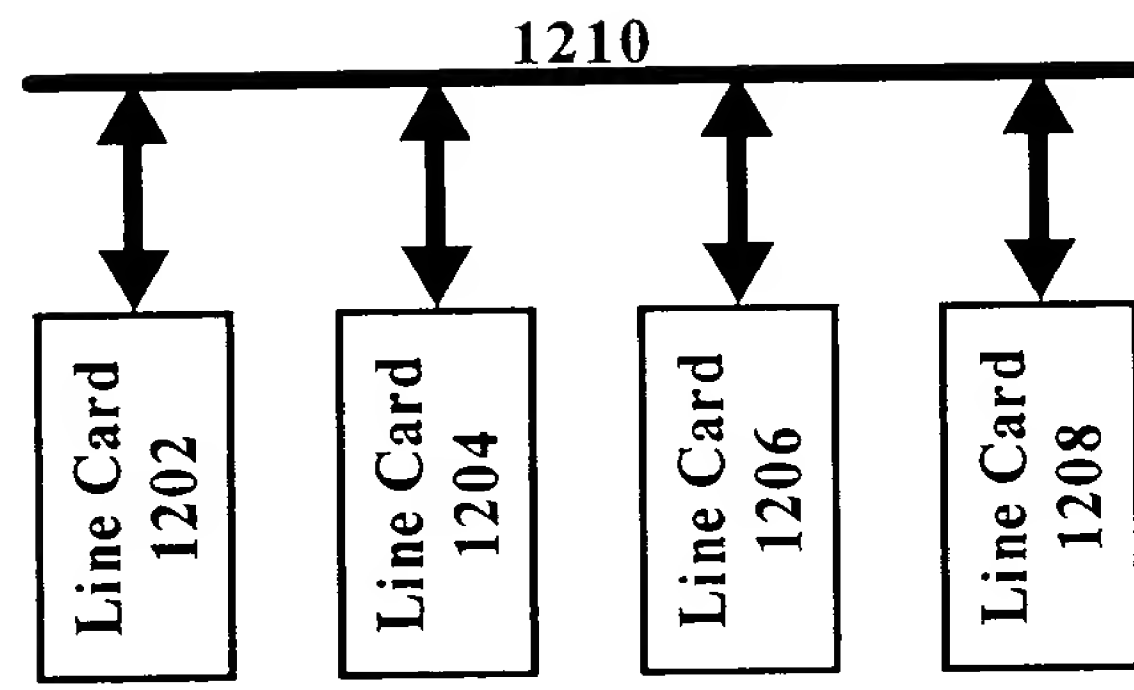


Fig. 12

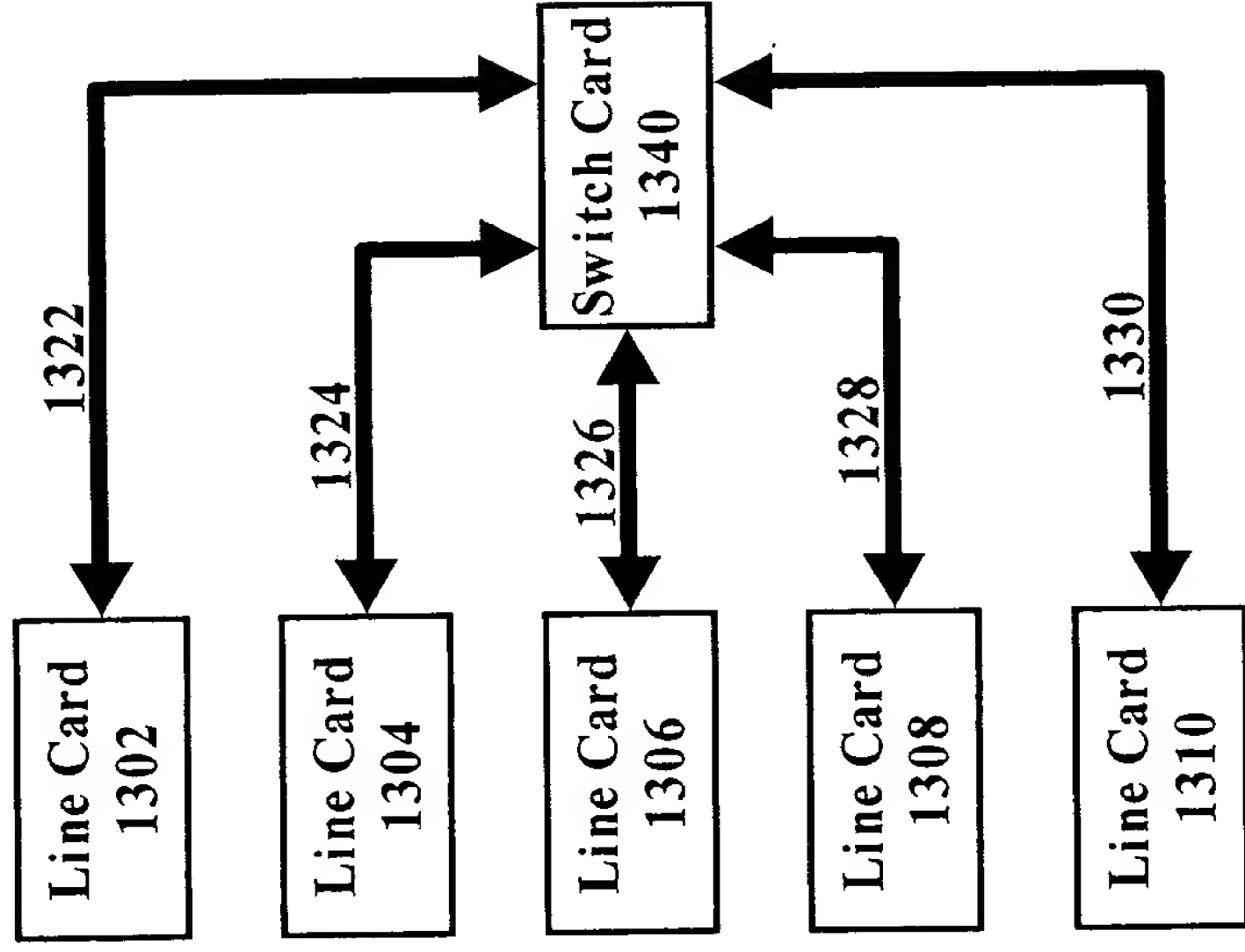


Fig. 13

